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Applicant: Pascal OUDET	)	Group Art No.: 2181
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	)	Examiner: Xuong M. Chung-Trans
	)	
Application No: 09/247,795	)	**RESPONSE TO FINAL REJECTION**
	)	
Filed: February 8, 1999	)	Our Ref: B-3604 616923-4
	)	
For: "Address Remapping For a Bus"	)	Date: April 11, 2002

Honorable Commissioner of Patents and Trademarks
Washington, D.C. 20231

Dear Sir:

This paper is filed in Response to the Official Action dated November 23, 2001. A request for a two-month extension of the time for responding to the Official Action accompanies this Response.

The Examiner continues to reject claims 1-8 and 10-17 based on 35 U.S.C. 102(e). These grounds for rejection are respectfully traversed.

The Examiner asserts, in the Final Rejection, that the cited prior art, the patent that Blackledge, works "bi-directionally." First, it is not enough that Blackledge "work" bi-directionally, but rather, that the address remapping occur bi-directionally as required by claims 1 and 16 and that the other limitations of these claims be fully met.

With respect to address remapping, the Examiner points to Figure 2 of Blackledge. Figure 2 of Blackledge is undeniably a one way address remapper given the fact that the address comparator and range filter 52 only samples one bus, namely PCI bus 56. There is no address comparator

and range filter for micro-channel bus 58. In a similar vein, in Figure 2, the translator 54, only translates addresses from bus 56 to new addresses on bus 58. There is no way for translation to work in the other direction. It is undeniable that the structure shown in Figure 2 provides a uni-directional address translation function.

The Examiner asserts, however, that the Blackledge system "must work bi-directionally" the Examiner pointing to column 5, lines 14-26 and columns 6, lines 1-2 of the Blackledge patent.

Before delving into the passages cited by the Examiner, it would be helpful to first look at Figure 1 of Blackledge. The Blackledge includes a host or primary bus 16 which interfaces with system memory 14. Of course, the address space which is addressable depends upon the number of bits available on the address bus from the CPU and those skilled in the art realize that the system memory seldom, if ever, occupies all of the address space. Part of the address space, instead of being dedicated to system memory, is dedicated to various hardware functions. The host to PCI bridge 18 converts the processor-unique signals on bus 16 to standardized I/O signals on bus 19 and the subordinate buses, 23, 25, 29 and 39 which are designed in compliance with the PCI standard. The system disclosed in Figure 1 can support multiple expansion buses, including micro-channel (MC) or ISA buses via a hierarchal bus structure. The element to which the Examiner refers to in Figure 2 allows communication between a PCI bus 56 and a micro-channel bus 58, and therefore corresponds to a bridge, such as bridge element 36, shown in Figure 1.

It is clear that the CPUs can address the hardware attached to a MC or ISA bus, for example, via bridges 28, 24 and 36. However, that addressing is strictly one way. The CPU could also address, for example, a PCI attached device 20, via bridge 18. That addressing is also one way.

In order to meet claim 1, the Examiner would have to at least show a bi-directional address re-mapper which is capable of accommodating a bus having two sections with each section of the

bus having at least one station which has a physical address, wherein the station on each section of the bus is assigned a dummy address for being addressed by a station on the other section, the address remapper remapping a dummy address from one section to a physical address on the other section. In terms of Figure 1 of the Blackledge patent, the Examiner would have to show, *inter alia*, a device attached to bridge 38 with a dummy address which could address a device attached to, for example, bridge 48, and vice versa so that the device attached to bridge 40 could also address the device attached to bridge 36. No such addressing occurs in Blackledge. All of the addressing appears to be done by the CPU and therefore is uni-directional. Of course, the data moves across the bridges bi-directionally, but the addressing occurs in one direction only. This fact is in concert with the observation that the bridge shown in Figure 2 only supports one-way address remapping. You cannot have dummy addresses on both sections of the bus as specifically required by claims 1 and 16 using the hardware of Figure 2.

Turning now to the discussion at column 5, it would be helpful to start the review at line 10 which indicates that the bridge is a "processor to host bus" bridge. Clearly, the addressing is emanating from CPU 12 in Blackledge. The address emitted by the processor must be properly directed through the bus structure to the correct destination, either an I/O device (via a bridge) or to a memory location in memory 14. When a bridge recognizes addresses which are assigned to its subsidiary bus, then the bridge responds on the bus with a device select signal (which is data!) indicating that the address has been accepted in a one way direction from the microprocessor to the device and that the device will respond. There is nothing whatsoever in the disclosure referenced by the Examiner to suggest that the addressing occurs bi-directionally.

Turning now to the passage at column 6, lines 1-2, the Examiner makes reference to a statement in the middle of a paragraph bridging columns 5 and 6. The references to memory address and I/O addresses is very clear. Turning again to Figure 1, the I/O addresses occur on PCI bus 19 whereas the memory addresses occur on host bus 16. Those skilled in the art will appreciate that

the host to PCI bridge 18 is only responsive a relatively small amount of the address space available on host bus 16. Most of the address space available on host bus 16 would be assigned to system memory 14. For example, the bottom 1MB of the address space might be assigned to hardware via the host to PCI bridge 18, while all addresses above that level might be assigned to system memory 14. The reference to memory to I/O or I/O to memory is clearly a reference to host to PCI bridge 18 since that is the only place that I/O 19 and memory bus 16 data transitions occur. Obviously, those skilled in the art would not assign system memory and hardware to common addresses, because that just results in inefficient utilization of system memory. Thus, the limitation regarding assigning a dummy address is not met at bridge 18. No dummy addresses are needed since there is no suggestion that the memory addresses overlap with the addresses assigned to hardware. Moreover, it is submitted that there is nothing in this disclosure which indicates that any address translation occurs in bridge 18, even uni-directionally! The address translation occurs in the device shown in Figure 2, which is the bridge between a PCI bus and a micro-channel bus, such as bridge 36, and not at bridge 18. It is submitted that bridge 18 only responds to address queries within the range of the hardware addresses on bus 16. Memory 14 responds (if it is available) to address inquires outside that range. With respect to the micro-channel bridge 36, that bridge clearly remaps addresses only uni-directionally as clearly shown by Figure 2.

The long and the short of it is that the message at column 6, to which the examiner refers, ia utterly irrelevant to the apparatus shown in Figure 2. The discussion at that point is with reference to a completely different bridge bridge 18). Those skilled in the art will appreciate the fact that no dummy addressing occur at that bridge.

Claim 1 clearly requires that a station on one station of the bus be assigned a dummy address for being addressed by a station on the other section of the bus. In Blackledge, all of the addressing is done by the CPU. There is nothing in Blackledge to suggest that a station, which must have its

own dummy address (in order to meet that limitation of claims 1 and 16), can address another station on a second portion of the bus which another station also has its own dummy address. That functionality is just not shown in Blackledge! The rejections of the claims under 35 USC 102(e) are improper and the Examiner is respectfully requested to withdraw them.

If the Examiner refuses to withdraw this rejection, then the Examiner is respectfully requested to explain in detail where each and every limitation of each and every rejected claims can be found in the Blackledge patent. For example, if the Examiner intends to continue to cite Figure 2 of Blackledgge as being anticipatory of the claimed invention, then the Examiner is requested to spell out exactly where there is disclosure in Blackledge of the two stations on either section of the bus as claimed in claims 1 and 16. Then, after identifying those two stations, the Examiner is respectfully requested to identify where it is disclosed that "each station in each section of the bus is assigned a dummy address for use when being addressed by a station on the other bus section..."

It is noted that the dependent claims include additional features which the Examiner has failed to make any real attempt at showing where the claimed features can be found in Blackledge. For example, claim 5 recites that the bus is a two wire serial bus. The examiner asserted in the official action dated dated May 24, 2001 that "the bus as disclosed in Blackledge et at is a conventional two wire bus with one wire ...". Is the Examiner asserting that the PCI and microchannel busses of Figure 2 are two wire busses? Is there any support for that assertion in the Blackledge patent? If so, the examiner is kindly requested to disclose where that support for that asserftion might be found. In the meantime, the Examiner might wish to review the enclosed article entitled "Creating a Third Generation I/O Interconnect" which is apparently published by Ajay V. Bhatt of Intel Corporation. It is currently available on the Internet at www.controlled.com/pci/faq.html. Note the discussion about the PCI bus being a "mult-drop, parallel bus implementation" on page one of that article.

If the Examiner refuses to withdraw the rejection, then the Examiner is respectfully requested to specificy, as nearly as possible, where each and every limitation of the claims can be found in Blackledge as required by 37 CFR 1.104(c).

The rejection made by the Examiner is under 35 USC 102. According to MPEP § 2131, a "claim is anticipated only if each and every element as set forth in the claim is found, either expressly or inherently described, in a single prior art reference," quoting *Verdegaal Bros v. Union Oil Co. of California*, 814 F.2d 628, 631 (Fed. Cir. 1987). Since Blackledge does not disclose all of the elements of claim 1 or all of the elements of claim 16, the Applicant resepctfully submits that both claims 1 and 16 of the present application are patentable over Blackledge. The dependent claims are also patentable over Blackledge, at least by virtue of their dependency from the independent claims.

The Applicant should not be placed in a position of having to speculate by the claims are being rejected. Since the Examiner has failed to met the burden of 35 USC 102 and MPEP § 2131, the rejection under 35 USC 102 must fail.

These comments largely reiterate the comments made by the undersigned during a telephone interview on April 8, 2002 with the Examiner and her Supervising Examiner, Mr. Peter Wong. The Examiners are thanked for giving applicant's attorney an opportunity to discuss this application with the Examiner and the Supervising Examiner. At the conclusion of the interview, the Supervisinng Examiner requested that written remarks be filed. That has now been done.

Reconsidcration of this Application is respectfully requested.

The Commissioner is authorized to charge any additional fees which may be required or credit

overpayment to deposit account no. 12-0415. In particular, if this response is not timely filed, the Commissioner is authorized to treat this response as including a petition to extend the time period pursuant to 37 CFR 1.136 (a) requesting an extension of time of the number of months necessary to make this response timely filed and the petition fee due in connection therewith may be charged to deposit account no. 12-0415.

I hereby certify that this correspondence is being sedut by facsimile to: Commissioner of Patents and Trademarks, Washington, D.C., 20231 at 703-746-72392 on

April 11, 2002
(Date of Deposit)

RICHARD P. BERG
(Name of Applicant, Assignee or Registered Representative)

(Signature)

April 11, 2002
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Respectfully submitted,

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